



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,447	10/26/2004	Hiroshi Takahara	260903US2PCT	4248
22850	7590	08/21/2009		
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P. 1940 DUKE STREET ALEXANDRIA, VA 22314				
EXAMINER				
CHOWDHURY, AFROZA Y				
ART UNIT		PAPER NUMBER		
2629				
NOTIFICATION DATE		DELIVERY MODE		
08/21/2009		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com

oblonpat@oblon.com

jgardner@oblon.com

Office Action Summary

Application No.

10/511,447

Applicant(s)

TAKAHARA ET AL.

Examiner

AFROZA Y. CHOWDHURY

Art Unit

2629

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 July 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8 and 10-21 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 11-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-7,10 and 15-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
- Paper No(s)/Mail Date 12/30/2008
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's request for continued examination (RCE) filed on **July 10, 2008** has been entered. Claims 1, 2, 4-8, and 10-21 are currently pending. As per last office action, claims 8 and 11-14 are withdrawn from further consideration as being drawn to nonelected groups. The restriction requirement is made Final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4-7, 10, and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sekiya et al.** (US Patent 6,583,775) in view of **Inoue et al.** (US Pub. 2002/0126107).

As to claim 1, Sekiya et al. discloses a drive method for an EL display panel, the EL display panel comprising:

EL elements (fig. 5(OLED)) arranged in a matrix (fig. 2);

driver transistors (fig. 5(TFT2)) which supply current to be passed through the EL elements (fig. 5(OLED), col. 13, line63 - col. 14, line 18);

first switching elements (fig. 5(TFT3)) placed in current paths of the EL elements (fig. 5, col. 13, line63 - col. 14, line 18); and

a gate driver circuit (fig. 2(21)) which turns on and off the first switching elements (fig. 5(TFT3)) for control (col. 13, line63 - col. 14, line 18);

wherein the gate driver circuit controlling the first switching elements in an off state two or more times during one frame period (fig. 5, col. 13, line63 - col. 14, line 18); and

an operation for retaining an image signal applied to each pixel is executed only once during the one frame period (col. 16, line 66 – col. 17, line 28).

Sekiya et al. does not explicitly teach generating a plurality of stripe non-display areas on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit.

Inoue et al. teaches generating a plurality of stripe non-display areas on a display screen and moving the plurality of stripe non-display areas in a scanning direction of the gate driver circuit (fig. 6, 7, [0078] – [0079]).

Therefore, it would have been obvious to one skill in the art at the time of the invention was made to modify the drive method for an EL display of Sekiya et al. incorporating the idea of Inoue et al. of generating and moving a plurality of stripe non-display areas on a display screen in a scanning direction in order to reduce power consumption and prevent flicker on a screen.

Claim 2 is rejected the same as claim 1 above.

As to claim 4, Sekiya et al. teaches a drive method for the EL display panel wherein the first switching elements are turned off periodically during one frame period (fig. 5, col. 13, line 63 - col. 14, line 18).

Claim 5 is rejected the same as claim 1 above, except:

first gate driver circuit (fig. 2(21)) and second gate driver circuit (fig. 2(23)).

As to claim 6, it is obvious to make an EL display panel where the first and second gate driver circuits are formed in a same process as the driver transistors and the source driver circuit is made of a semiconductor chip.

As to claim 7, Sekiya et al. discloses an EL display panel wherein the second gate driver circuit selects a plurality of gate signal lines and supplies the image signal to the driver transistors of a plurality of pixel rows (fig. 2).

As to claim 10, it is an obvious design choice to make an EL display panel wherein the gate driver circuit is constructed of p-channel transistors.

As to claim 15, Inoue et al. teaches an EL display apparatus comprising: the EL display panel and a receiver (fig. 17).

As to claims 16 and 17, Sekiya et al. teaches a drive method for the EL display panel wherein the driver transistors are P-channel transistors (fig. 12).

As to claims 18 and 19, Sekiya et al. teaches an drive method for the EL display panel wherein brightness of the display screen is varied or controlled by varying proportion of the non-display area to a display area of the display screen (col. 4, lines 4-14, 42-49, col. 13, lines 60-67).

Claim 20 is rejected the same as claim 16 above.

Claim 21 is rejected the same as claim 10 above.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 2, 4-7, 10, and 15-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AFROZA Y. CHOWDHURY whose telephone number is (571)270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC
8/13/2009

/Bipin Shalwala/
Supervisory Patent Examiner, Art
Unit 2629